UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/477,217	01/04/2000	RONALD ALAN RUSSELL	M-7269-US	8864

33031 7590 03/25/2004

CAMPBELL STEPHENSON ASCOLESE, LLP
4807 SPICEWOOD SPRINGS RD.
BLDG. 4, SUITE 201
AUSTIN, TX 78759

EXAMINER	
PHAN, TRI H	

ART UNIT	PAPER NUMBER
2661	10

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/477,217	RUSSELL ET AL.	
	Examiner	Art Unit	
	Tri H. Phan	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33-37* is/are allowed.

6)☒ Claim(s) *1-5,8,9,20-22,24,25, 28-31 and 38* is/are rejected.

7)☐ Claim(s) *6,7,10-19,23,26,27 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Arguments

1. This Office Action is in response to the Response/Amendment filed on January 9th, 2004. Claims 1-38 are now pending in the application.

Drawings

2. The proposed drawings were received on July 22nd, 2003. The drawing of Figure 1B is disapproved by the examiner.

The drawing is objected to because all blocks in Figure 1B should be labeled with descriptive legends based on 37 C.F.R. § 1.84(o) for supporting the objection in the Rules and M.P.E.P.; For example, node 195 (1-9) should be labeled with descriptive legends as -- network node (or router) --, link 192 should be labeled with descriptive legends as -- physical path --, link 191 should be labeled with descriptive legends as -- virtual path --, etc.. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 2 is objected to because of the following informalities:

In claim 2, it recites the limitation "*said switching matrix is configured to identify said switching matrix ...*" in line 4; that is vague and unclear to which switching matrix it refers to the

"switching matrix" in the parent claim, i.e. claim 1; or the "switching matrix" of the plurality of switching matrices as defined in claim 2, line 6. Examiner interprets the claim language as referring to --- other switching matrix is configured to identify said switching matrix ... --- for the purpose of further examination on the merits.

Applicant is required to provide appropriate correction.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 24 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Claim 24 recites the limitations "said framing error" in line 2. There is insufficient antecedent basis for this limitation in the claim 24. The ""said framing error"" is not defined within Claim 24 nor in the parent claim (claim 20).

- Claim 25 recites the limitations "said error checker" in line 1. There is insufficient antecedent basis for this limitation in the claim 25. The "said error checker" is not defined within Claim 25 nor in the parent claim (claim 20).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-5, 20-21, 28-30 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by **Shiragaki** (U.S.5,457,556).

- In regard to claims 1, 20 and 28, **Shiragaki** discloses in Figs. 2-3, 5, 8-13 and in the respective portions of the specification about the system and method for minimizing the fault recovery procedures of the optical cross-connect system of the network center and the network nodes ("*signal router*") having optical space switch ("*switch matrix*"), wavelength-divided space switch and time switch with inputs and outputs ("*switch matrices*") (For example see Figs. 1-3, 5, 8-9 and 11; col. 4, line 54 through col. 5, line 26); wherein the optical cross-connection system has main and auxiliary fault detectors ("*error detector*"; For example see Figs. 2, 9 and 11) for collecting data, detecting line fault and link failure from all strategic points of the system (For example see col. 5, lines 50-62), and when the failure occurs, issuing ("*generating error information*") and sending the command signal("command") to the control circuit ("*controller*") or network center (It is inherent that the network center is used for controlling the whole system which is including a plurality of nodes as disclosed in col. 2, line 65 through col. 43, line 10) for

controlling and instructing the switch to switch from the faulty link or port to the spare link or port (For example see Figs. 2-3, 5, 8-9, 11 and 13; col. 5, line 62 through col. 8, line 7).

- Regarding claims 2-5, **Shiragaki** further discloses about the optical space switch, wavelength-divided space switch, time switch implementing with multiple stages ("*switch matrices*") (For example see Figs. 1-3, 5, 8-9 and 11; col. 4, line 54 through col. 5, line 26) controlling by the control circuit or network center to change from the faulty link or port to the spare link or port; and where the fault detector detects the failure at different strategic points of the system, issues and sends the switching command signal to the control circuit or network center for controlling and instructing the switch to switch from the faulty link or port to the spare link or port as claimed in the claimed invention 2 (For example see Figs. 2-3, 5, 8-9; col. 6, line 5 through col. 8, line 7; col. 8, line 49 through col. 10, line 51); wherein the main fault detector ("*error detector*") is connected to the inputs and outputs of the space switch and the auxiliary fault detector ("*error detector*") is connected to the inputs and outputs of the wavelength switch and time switch to detect the faults and report to the control circuit or network center for switching between the switches as claimed in the claimed inventions 3-5 (For example see Figs. 11 and 13; col. 10, lines 52-62; col. 11, line 28 through col. 12, line 8).

- In regard to claims 21, 29-30 and 38, **Shiragaki** further discloses about the controller and the network center in the network management system control the switches for switching between the faulty channels or input/output ports detecting by the fault detector (For example see col. 6, line 5 through col. 8, line 7).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Shiragaki** (U.S.5,457,556).

- In regard to claims 8-9, **Shiragaki** discloses all the subject matter of the claimed invention as discussed in part 7 of this Office action above, about the system and method for minimizing the fault recovery procedures of the optical cross-connect system of the network center and the network nodes ("*signal router*") having optical space switch ("*switch matrix*"), wavelength-divided space switch and time switch with inputs and outputs ("*switch matrices*"); wherein the optical cross-connection system has main and auxiliary fault detectors ("*error detector*") for collecting data, detecting line fault and link failure from all strategic points of the system, and when the failure occurs, issuing and sending the command signal to the control circuit ("*controller*") or network center for controlling and instructing the switch to switch from the faulty link or port to the spare link or port. **Shiragaki** does disclose about the time switch with the time-division multiplexers and demultiplexers ("*demultiplexer*") connecting to the auxiliary fault detector ("*error detector*") and the time slot interchangers 'TSI' ("*clock and data*

recovery unit") to recover for the fault that occurs in the time slot of any time slot interchangers (For example see Figs. 9-10; col. 9, line 5 through col. 10, line 51); but fails to specifically disclose about the "phase-lock loop". However, using the "phase-lock loop" is well known in the art for correcting the phase or time of the faulty signal in the telecommunication and **Shiragaki** also discloses the use of the digital switch for looping the signal from output port back to the input port of the time switch (For example see col. 9, line 14-23). Therefore, it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the phase-look loop for correcting the phase or time of the faulty signal and loop back the signal from output port to input port for correcting as disclosed in the loop back signal of the digital switch of **Shiragaki**'s system.

10. Claims 22 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Shiragaki** (U.S.5,457,556) in view of **Al-Salameh** (U.S.6,262,820).

- In regard to claims 22 and 31, **Shiragaki** discloses all the subject matter of the claimed invention as discussed in parts 7 and 9 of this Office action above, about the system and method for minimizing the fault recovery procedures of the optical cross-connect system of the network center and the network nodes ("*signal router*") having optical space switch ("*switch matrix*"), wavelength-divided space switch and time switch with inputs and outputs ("*switch matrices*"); wherein the optical cross-connection system has main and auxiliary fault detectors ("*error detector*") for collecting data, detecting line fault and link failure from all strategic points of the system, and when the failure occurs, issuing and sending the command signal to the control

circuit ("*controller*") or network center for controlling and instructing the switch to switch from the faulty link or port to the spare link or port. **Shiragaki** further discloses about the main fault detector with the diagnostic circuit for monitoring all possible faulty conditions, determining whether the trouble is and reports to the network center as well as the controller (For example see col. 10, line 63 through col. 11, line 18); but fails to specifically disclose about the "error counter". However, such implementation is known in the art.

For example, **Al-Salameh** discloses in Figs. 1-2 and 4-5 and in the respective portions of the specification that the optical node ("*signal router*"), which uses to route the transmission media ("*information stream*"), comprises a switch matrix ("*switching matrix*") having a plurality of inputs A-H for receiving transmission channel inputs ("*optical receivers*") and a plurality of outputs I-N ("*optical transmitters*") as disclosed in Col. 5, Lines 61-66; optical monitor ("*receiver error detector*") for detecting the presence or absence of input optical signal ("*errors in the information stream*") in transmission channels, generating indications and supplying the switch control signals CS ("*error information*") to the sub-controller and then to the optical switch matrix as disclosed in Col. 4, Line 66 through Col. 5, Line 12; and a main controller ("*controller*"), when receiving the CS ("*error information*"), selects an input from the plurality of inputs to an output from the plurality of outputs (For example see Figs. 4-8; Col. 5, Lines 17-37; Col. 7, Lines 23-30). **Al-Salameh** also discloses the switch matrix restores the failure by the indicating switch control SC signal set and reset ("*clearing error counter and starting error timer*") by the counter clock ("*clock and data recovery unit*") when the threshold ("*terminal value*") has been reached as disclosed in Fig. 9; Col. 9, Line 34 through Col. 10, Line 16; and the

add/drop multiplexer ("*demultiplexer*") as disclosed in Figs. 2 and 12; Col. 4, Line 17 through Col. 5, Line 60.

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to implement the counter clock in the optical communication system as taught by **Al-Salameh** in the **Shiragaki**'s main fault detector, with the motivation being to improve the ability to control the faulty time and limit with the counter clock with threshold in detecting faulty error.

11. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Shiragaki** (U.S.5,457,556) in view of **Upp et al** (U.S.4,967,405).

- In regard to claims 24-25, **Shiragaki** discloses all the subject matter of the claimed invention as discussed in parts 7 and 9 of this Office action above, about the system and method for minimizing the fault recovery procedures of the optical cross-connect system of the network center and the network nodes ("*signal router*") having optical space switch ("*switch matrix*"), wavelength-divided space switch and time switch with inputs and outputs ("*switch matrices*"); wherein the optical cross-connection system has main and auxiliary fault detectors ("*error detector*") for collecting data, detecting line fault and link failure from all strategic points of the system, and when the failure occurs, issuing and sending the command signal to the control circuit ("*controller*") or network center for controlling and instructing the switch to switch from the faulty link or port to the spare link or port. **Shiragaki** also discloses about the faulty error in loss of signal ("*loss-of-signal error*") detecting by the fault detector (For example see col. 7, line

3-11) in the optical cross-connect system ("*SONET*") as claimed in the claimed invention 24. **Shiragaki** further discloses about the main fault detector with the diagnostic circuit ("*error checker*") for monitoring all possible faulty conditions, determining whether the trouble is and reports to the network center as well as the controller (For example see Fig. 12; col. 10, line 63 through col. 11, line 18); but fails to specifically disclose about the "*parity checker*" and "*parity error*". However, such implementation is known in the art.

For example, **Upp** discloses in Figs. 2b and 6 and in the respective portions of the specification about parity error circuit ("*parity checker*") checks the parity error ("*parity error*") of the SONET signal based on the loss of signal, frame, or pointer for the cross-connection system (For example see col. 9, line 48-62; col. 11, lines21-40; col. 13, lines 40-59).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to implement the parity error circuit in the optical cross-connection system as taught by **Upp** in the **Shiragaki**'s main fault detector, with the motivation being to improve the ability to detect parity error in the transmitting frames.

Allowable Subject Matter

12. Claims 6-7, 10-19, 23, 26-27 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Claims 33-37 are allowed.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ishiwatari (U.S.5,446,725), **Watanabe et al.** (U.S.6,246,665) and **Mochizuki et al.** (U.S.6,674,714) are all cited to show devices and methods for improving switch's error detection communication architectures, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan, whose telephone number is (703) 305-7444. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Olms can be reached on (703) 305-4703.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 305-3900.

Tri H. Phan
March 12, 2004